Cont A1

forming a plurality of inter-metal dielectric layers on the substrate, wherein at least one inter-metal dielectric layers layer among the plurality of the inter-layer dielectrics has a silicon carbide layer of about 100Å to about 1000Å thick formed thereon.

A2

8. (Once amended) A method for fabricating a flash memory, comprising the steps of:

forming a stacked gate structure and a source/drain on a substrate;

forming an inter-layer dielectrics on the substrate; and

forming a silicon carbide layer of about 100Å to about 1000Å thick on the inter-layer dielectrics.

A3

13. (Once amended) A method for fabricating a flash memory, comprising the steps of:

forming a stacked gate structure and a source/drain on a substrate;

forming an inter-layer dielectrics on the substrate;

forming a contact in the inter-layer dielectrics;

forming a metal interconnection on the inter-layer dielectrics;

forming an inter-metal dielectrics on the substrate; and

forming a first silicon carbide layer of about 100Å to about 1000Å thick on the inter-metal dielectrics.

Please cancel claims 2, 9 and 14 without prejudice or disclaimer.

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Present Status of the Application

This Amendment is promptly filed to place the above-captioned case in condition for allowance. Claims 1, 8 and 13 have been amended. An annotated version of claims 1, 8 and 13 illustrating the changes made thereto is attached hereto as Exhibit A. The amendments made to the independent claims 1, 8 and 13 are for clarification and proper interpretation of the claims as we set forth in our specification and are well support by the specification. Claims 2, 9 and 14 have been canceled without prejudice or disclaimer. No new matter has been added to the application by the amendments made to the claims or otherwise in the application. For at least the following reasons, it is submitted that this application is in condition for allowance. Reconsideration and withdrawal of the Examiner's rejection is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 1-20 under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA hereinafter) and Xing (US 6,492,222).

Claims 1, 8 and 13 stand rejected under 35 U.S.C. 103(a) as purportedly being unpatentable over AAPA and Xing. As described in detail hereinafter, Applicant has amended claims 1, 8 and 13 and respectfully asserts that the rejection is no longer proper.

In accordance to the teaching of the present invention, a thin silicon carbide layer is formed on at least one layer of the plurality of the inter-layer dielectrics. The thin silicon carbide layer of the present invention is about 100 angstroms to about 1000 angstroms thick. The thin but with an adequate thickness silicon carbide layer formed on the inter-layer dielectrics can absorb UV irradiation effectively and block mobile ions in the following processes. Further, the

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thin silicon carbide layer can smooth out the microscratches formed on the inter-layer dielectrics after the CMP process to improve the yields. Beside, since the silicon carbide layer is only about 100 angstroms to about 1000 angstroms thick, it has a lesser impact on the overall dielectric constant of the inter-layer dielectrics (the dielectric constant of SiC can be as high as 6.5 to 9.7). Xing, on the other hand, teaches that the interlevel dielectric layers 112, 134 and 160 are comprised of a list of materials that include silicon carbide. An inter-layer dielectrics is typically about 4000 Å to 120000Å thick (cited reference Udea US2002/0115310, USP 6,277765, USP 6137176, etc.). In summary, the silicon carbide layer of the present invention basically serves as a cap layer for the interlayer dielectrics, and its thickness is thereby only in the order of hundreds of angstrom, whereas the silicon carbide of Xing is served as the interlayer dielectrics having a thickness of at least thousands to tens of thousands angstroms. When combining AAPA with Xing, an interlayer dielectrics that comprises silicon carbide or a silicon carbide interlayer dielectrics, having a thickness of at least above 4000 Å, is resulted. Therefore, the combination of AAPA and Xing fails to teach or suggest a thin layer of silicon carbide of about 100Å to 1000Å is formed on an interlayer dielectrics, in which UV radiation is effectively absorbed without adversely affecting the overall dielectric constant. For at least these reasons, Applicant respectfully asserts that claims 1, 8 and 13 and claims 3-7, 10-12 and 15-20 which utilize claims 1, 8 and 13, respectively, as a base claim patentably define over AAPA and Xing. Reconsideration and withdrawal of this rejection on the now pending claims are respectively requested.

CONCLUSION

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For at least the foregoing reasons, it is believed that the presently pending claims 1-20 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims

Please amend the following claims:

1. (once amended) A method for fabricating a flash memory, comprising the steps of:

forming a stacked gate structure and a source/drain on a substrate;

forming an inter-layer dielectrics on the substrate; and

forming a plurality of inter-metal dielectric layers on the substrate, wherein at least one inter-metal dielectric layers layer among the plurality of the inter-layer dielectrics [and the inter-metal dielectric layers] has a silicon carbide layer of about 100Å to about 1000Å thick formed thereon.

8. (Once amended) A method for fabricating a flash memory, comprising the steps of:

forming a stacked gate structure and a source/drain on a substrate;

forming an inter-layer dielectrics on the substrate; and

forming a silicon carbide layer of about 100Å to about 1000Å thick on the inter-layer dielectrics.

13. (Once amended) A method for fabricating a flash memory, comprising the steps of:

forming a stacked gate structure and a source/drain on a substrate;

forming an inter-layer dielectrics on the substrate;

forming a contact in the inter-layer dielectrics;

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forming a metal interconnection on the inter-layer dielectrics;

forming an inter-metal dielectrics on the substrate; and

forming a first silicon carbide layer of about 100Å to about 1000Å thick on the inter-metal dielectrics.

Please cancel claims 2, 9 and 14 without prejudice or disclaimer.

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